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TECHNICAL MEMORANDUM (NASA) 25

NARROW BAND BINARY PHASE LOCKED LOOPS

Very high Q digital filtering circuits for audio frequencies in the range of 1 Hz to 15 KHz are implemented in simple CMOS hardware using a binary local reference clock frequency. The circuits have application to VLF navigation receivers and other narrow band audio range tracking problems.

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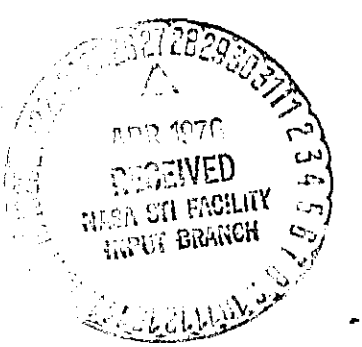

I. INTRODUCTION

A first order digital phase lock loop, where gated binary frequencies of 2^i and 2^{i-1} are equivalent to the VCO of an analog PLL, provides tracking over a 2:1 input frequency range. The BPLL operates best as a narrow band tracking loop where the input signal is prefiltered by analog means and approximately centered between the upper and lower limits. The precision of replicating the input signal is proportional to a multiplying factor k, where a binary divider chain of k bit length generates the output frequency from reference clocks of 2^{i+k} and 2^{i+k-1}, respectively. Thus, the positive edge to positive edge variation of the output frequency can be specified to within k bits for any given case.

II. SINGLE TRACKING LOOP CIRCUIT

A 3-chip hardware implementation of the basic circuit is illustrated in Figure 1, where a two phase input signal is fed to a pair of EXOR gate phase detectors. The output locked estimate is obtained by dividing by a binary number k which is sufficient to bracket the input frequency f (faster or slower) such that $2^i > f > 2^{i-1}$. Crystal controlled binary clock frequencies like 2^{15} Hz, commonly used as the input reference for digital wristwatches, provide a convenient clock source for low audio frequency tracking in the 1 to 500 Hz range.

III. DUAL FREQUENCY TRANSLATION LOOP

A digital superheterodyne method, where the input signal is first mixed with a binary local oscillator in a type D flip-flop, is used to provide narrow band tracking at higher input frequencies from the same 2^{15} Hz binary clock reference. The input signal f is first mixed with a L.O. frequency of 2^n Hz, where n is an integer and m is a harmonic of the LO that is near the input signal frequency, according to the relation: $f - m \cdot 2^n - 2^n = IF$ (Intermediate Frequency).

For the case where the input f is 10,200 Hz, the resulting IF is 40 Hz with an effective LO of 2048 Hz where $n = 11$ and $m = 4$. The translation loop circuit of Figure 2 is an example where the inner loop $k = 9$, and the outer loop $k = 4$. The effective tracking bandwidth of this system is $IF/2^4$ or 2.5 Hz at the center frequency. Thus a 10,200 Hz noisy input signal can be tracked with an effective "Q" of 4000 at a lower translated frequency. Longer integration times or larger filtering factors may be used in these types of loops with a higher reference frequency clock (i.e > 2^{15} Hz) and dividing by larger k factors to provide the same bit precision but at a narrower output bandwidth.

IV. APPLICATIONS

These BPLL methods have been applied to VLF (very low frequency) navigation receivers operating in the 10 KHz to 15 KHz region. They are of particular value in generating very narrow band replicas of noisy input signals when the input frequency is known. They have also been applied to tracking of subaudio frequencies like 8 Hz.

A memory aiding feature may be added by using a presettable counter for the output divider chain and loading the counter with the previous loop phase estimate. An asymmetric binary estimate of the loop phase is obtained from the Q outputs of the counter chain. The memory periodically loads this previous estimate of the phase position into the counter in sampled type systems where the input signal is multiplexed between several channels.

Virtually any low frequency may be tracked by choosing a reference clock rate such that there are an integral number of clock pulses faster or slower than the desired output frequency for cases where a binary frequency clock is not convenient.

Similar methods are possible using other standard CMOS packages. For example, the CD4046 phase locked loop chip has a type II edge sensitive phase detector memory system which can generate gates proportional to > signal, = signal, or < signal. (The VCO part of the CD4046 is not used here.) A related circuit in TTL would involve the use of the MC4044 phase detector chip.

V. ACKNOWLEDGEMENT

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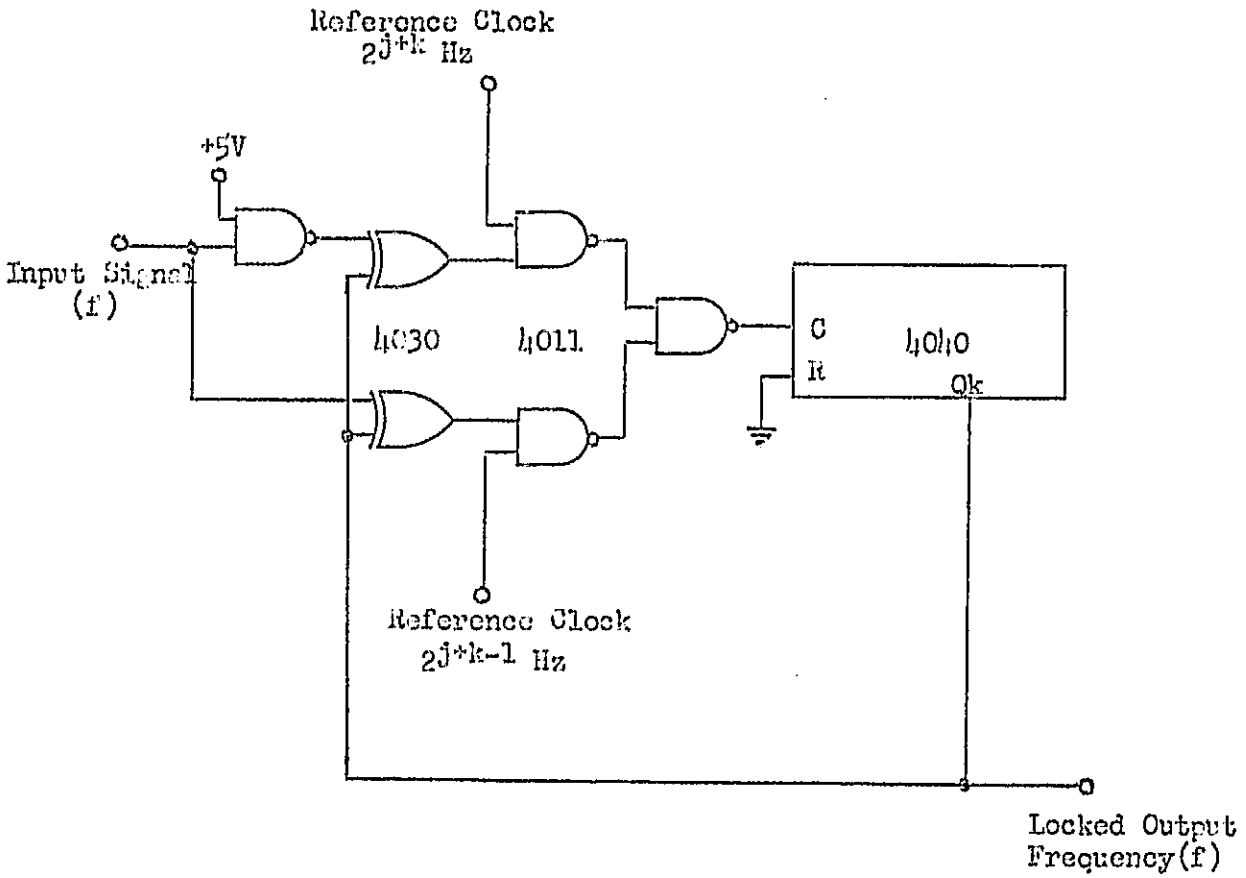

Figure 1. Binary Phase Locked Loop.

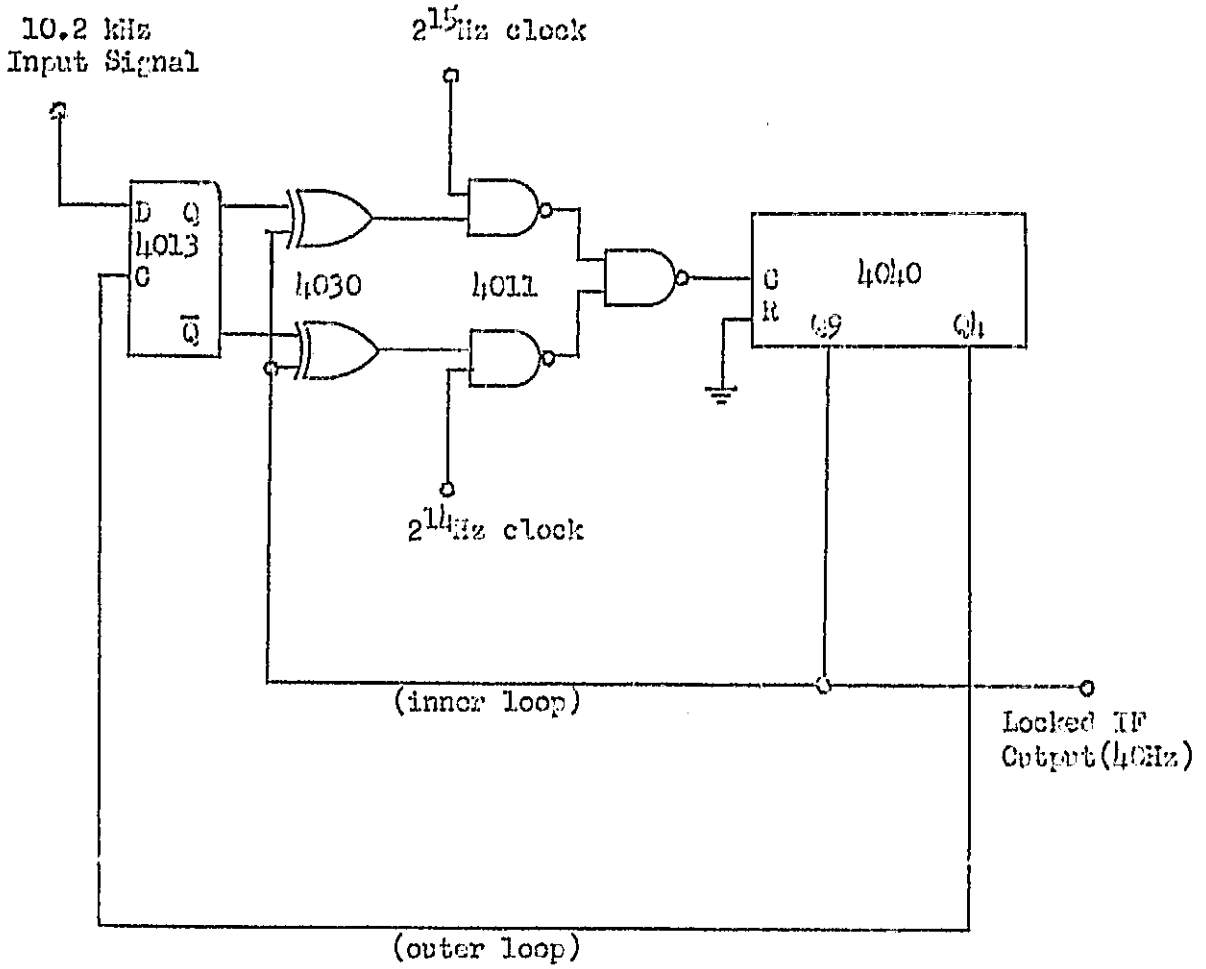

Figure 2. Binary Frequency Translation Loop.